THE INFLUENCE OF NON CURRICULAR COURSES ON UNDERGRADUATES' TECHNICAL PROFESSIONAL DEVELOPMENT

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Abstract *¾ New-technology extracurricular courses were offered to electronic engineering undergraduates. This experience permitted to verify how the students integrated them the with regular ones, and it also allowed evaluating the role of extra-curricular activities in preparing students for their future in industry. A conceptual 40-hour Hardware Description Language course, supported by the well-known semiconductors company Altera, was offered and 1/3 of the students enrolled. . As a result there was a change in the project methodology of electronic undergraduates, in designing programmable digital hardware, and a considerable increase in this kind of projects. It was noticed that extra-curricular technological courses can stimulate students to study and they open new perspectives in their professional activities. Students could perceive an opportunity for distinction among their colleagues and felt attracted by the possibility of effective industrial applications. Courses were successful also because of the industrial appeal, contributing with a more professional character, rather than an academic one.*

Index Terms ¾ VHDL courses, digital systems, final- course projects.

INTRODUCTION

Regular graduation courses at FEI-Faculdade de Engenharia Industrial, are planned to be concluded in a minimum of five or six years, depending on whether they are day or night courses, divided in ten or twelve-semester terms respectively, and have quite a rigid structure, with pre-determined semestral disciplines. Courses are based on an average of a 30 class/hour a week schedule, 40% of which is reserved to laboratory classes.

No elective disciplines are allowed to be taken by the students, so as to build their own plan of studies and substitute them with some of the subjects that make part of the regular curriculum.

Courses are divided in two main cycles, that is a four-semester propedeutic one, which is common to all engineering courses, and a six-semester professional one, for specific areas, such as Electrical, Chemical, Mechanical, Metallurgical, Civil and Textile Engineering. The choice of area is made during the fourth term, when the student will have to make his option for a specific carrier. Particularly, in the Electrical Area, possible options are Computer, Electronics, Telecommunications or Electrical-Production Engineering. The respective curricula can be seen on the site http: www.fei.br/eletrica.

The need for elective subjects was overcome with the offering of extra-curricular disciplines and courses along the year, and most frequently between academic terms. Private enterprises, with which FEI maintains partnership and the Program for Scientific Initiation would generally give full support for these courses, both with instructors, equipment, and even financial aid for the best students.

Another and new important alternative source for extra-curricular courses was given by the TQP-Technological Qualification Program, which was implemented at FEI in partnership with MOTOROLA [4], with excellent results. It should be pointed out that this successful outcome was due in part to the restrictive selection of students that was made. It was restrictive both regarding the necessary pre-requisites that were required to be apt to take the course adequately and with respect to the qualifying academic records of the student.

It had already noticed that the students in general responded better to extra-curricular courses than to formal academic ones: they had better performance, attended classes regularly and were genuinely interested in the course and pro-active. Many aspects were considered, such as specific interests, class didactics and dynamics, up-to-date topics, enterprise involvement, which would give more credibility for professional utility, trying to identify which would be more sensitive to provoke a change in attitude. An investigation was made among the students about this.

All of the aspects had a certain influence, still most characteristics were similar to those of regular courses, and they would not justify those results. The factors that were really distinguishing were, on one side, the interest for the subject the student had at that time, because they needed it, and on the other side, the sense of freedom and responsibility the students had, since they were not obliged to take the course to graduate, but rather acted with a professional attitude.

This suggested some faculty members of the Electrical Engineering Course that some of the regular technological courses might also be offered as extra-curricular courses, with the right support from companies clearly identified with the subject, to all students who might be interested.

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The initiative started from the necessity of investing in new technologies and alternative methods to be used in digital systems disciplines, at undergraduate level.

The way the course should be carried out should be different from the conventional one, allowing more freedom as to program contents, presence, timetable, evaluation, and stimulating creativity and new conditions for teacher-student approximation.

COURSE PROPOSITION

Motivation and Thematic

The choice of the subjects was also influenced by the material availability, such as software EDA, didactics kits and adequate bibliography, from the Altera Corp. University Program, and the need to start new project methodologies with undergraduate students.

The subject is related to the disciplines Digital Systems II, III, and I where conventional sequential digital circuits techniques are used, including Petri Nets and logic-schematic diagrams. The correspondent laboratory activities are based on standard SSI and MSI integrated circuits and EPLD's and FPGA's programmable logic devices, which should enable the students to design and implement any digital circuit.

The proposition of the course was teach a description alternative method, by means of VHDL-Very High Speed Integrated Circuit Hardware Description Language, which allows that sophisticated software tools to automate conventional and limiting manual techniques be used, the project objective be clearer than the corresponding schematic representation, simpler and clearer documentation generation of the system, and portability of the project to be compiled with other tools and technologies, according to [1], [2] e [3], besides the norms by IEEE-STD-1076/1987 and IEEE-STD-1164/1993, which established the international patterns for this language. These references were used as basic bibliography for the course.

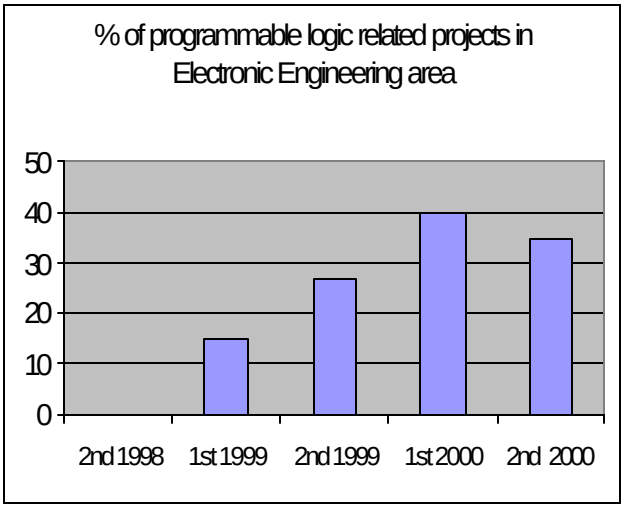
The VHDL Study Group was created for this initiative, so as to integrate teachers and students, and 1/3 of the potential interested ones showed up and took the course. Classes were in part theoretical and practical, with workgroups, hands on work, simulations and final implementation of individual projects.

INFLUENCE ON THE SCIENTIFIC INITIATION PROGRAM

When the VHDL Study Group was created it was expected that it would promote a transformation in the project methodology used by the scientific initiation program students, but what happened is that besides this there was an increase interest in the subject and a broader concern with the use of digital circuits in applied research. The SI (Scientific Initiation) students noticed that their activities had a differential aspect, maybe due to the influence of Altera University Program, which would lead not only to the academy but also to professional engineering placements.

The evolution of programmable logic interest in the last semesters in shown in figure 1

FIGURE 1
INCIDENCE EVOLUTION OF PROGRAMMABLE LOGIC



Besides the quantitative aspect there was also an increase in the degree of complexity in the digital systems contents.

An example of this is the work [5] briefly described hereafter, which deals with a pipeline architecture for FIFO memories. Some alternatives are presented and all were implemented and tested in FPGA's. The first is a high level description of a FIFO functioning with a CAE tool automatic implementation. The second includes a detailed read/write mechanism, with a cycle-share. The last one describes the pipeline mechanism which allows a quicker interface.

FIFO memories are sequential storing devices with possible multiple inputs and outputs, which work on a first-in-first-out basis, even at different read and write rates.

Listing 1 describes a FIFO memory implementation, with VHDL direct translation code with no circuit suggestion.

"Le" and "Escreve" are input signals responsible for memory read/write, whereas "Entrada" corresponds to data to be transferred. Output signals "Cheio"and "Vazio" correspond to the internal state of the contents, and they are used for flux control at the interface. Signal "Saida" receives the transferred data, whereas the "Quandt" function calculates the indicator values using the address pointers.

The code was compiled with the tools MaxPlus II, from Altera, and Foundation, from Xilinx, for components fitting, and although it seems to be simple, the solution it generated

was quite complex: even for small dimensions (32x8, 64x8) the automatic process synthesis took more then an hour. This fact indicates the need of the designer interference in the circuit solution, as it was done in the other two forms described hereafter.

LISTING 1
DIRECT IMPLEMENTATION

```
@@   @@   @@@@@@   @@       @@@@@@   @@@@@@   @@
@@   @@   @@   @@  @@       @@       @@       @@
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--Grupo de Desenvolvimento de Hardware Digital
--FEI - Faculdade de Engenharia Industrial
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================================================
--Projeto: Memória FIFO
--Paula G D Agopian
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LIBRARY IEEE;
USE IEEE.std_logic_1164.all;

ENTITY fifo_biba IS
        PORT(
                Clock, Le, Escreve: IN STD_LOGIC;
                Entrada: IN     STD_LOGIC_VECTOR(7
downto 0);
                Saida: OUT      STD_LOGIC_VECTOR(7
downto 0);
                Cheio, Vazio: BUFFER STD_LOGIC);
END fifo_biba;


--
================================================

ARCHITECTURE a OF fifo_biba IS
        CONSTANT Tamanho: Integer :=31; --
Profundidade da Memória

        SUBTYPE Palavra IS STD_LOGIC_VECTOR (7
DOWNTO 0);
        TYPE Memoria IS ARRAY (0 TO TAMANHO) OF
Palavra;

        SIGNAL Area: Memoria; --Define uma área de
memória Tamanho x 8
        --Ponteiros de Leitura e Escrita
        SIGNAL Conta_Leitura : Integer RANGE 0 TO
TAMANHO;
        SIGNAL Conta_Escrita : Integer RANGE 0 TO
TAMANHO;

--
================================================

        FUNCTION Quant (End_Le:
Integer;End_Es:Integer) return Integer is
        VARIABLE Volta: INTEGER RANGE 0 TO TAMANHO;
                BEGIN
                IF End_Es >= End_Le THEN
                        Volta := End_Es - End_Le;
                ELSE
                        Volta := 128 + End_Es -
End_Le;
                END IF;
            RETURN Volta;

        END Quant;

--
================================================

BEGIN
        PROCESS(Clock)
        BEGIN
        IF Clock'EVENT AND Clock ='1' THEN
                IF Escreve = '0' AND Cheio = '0'
THEN
                        Area(Conta_Escrita) <=
Entrada;
                        Conta_Escrita <=
Conta_Escrita + 1;
                END IF;
                IF Le = '0' AND Vazio = '0' THEN
                        Saida <=
Area(Conta_Leitura);
                        Conta_Leitura <=
Conta_Leitura + 1;
                END IF;
        END IF;
        END PROCESS;


        Vazio <= '1' WHEN
Quant(Conta_Leitura,Conta_Escrita) = 0 ELSE '0';
        Cheio <= '1' WHEN
Quant(Conta_Leitura,Conta_Escrita) = 127 ELSE '0';
END a;
```

In the cycle-shared implementation, the read/write mechanism must receive a clock signal with a frequency, which is the double of the system clock. which is a limitation for the maximum clock frequency will always be limited to half of that offered by the device technology.
Altera offers an application [6] for this solution, which can be used to test this technology.

The pipeline implementation is described as a data flow and a control machine, which determines the data transfer. The data flow structure is constituted of a two-block memory for data entry, two interface registers and one for output (figuere2). Four pointers, two for each memory block, take control of R/W (read/write) address. Other input signals allow write, read, or both simultaneously, request.

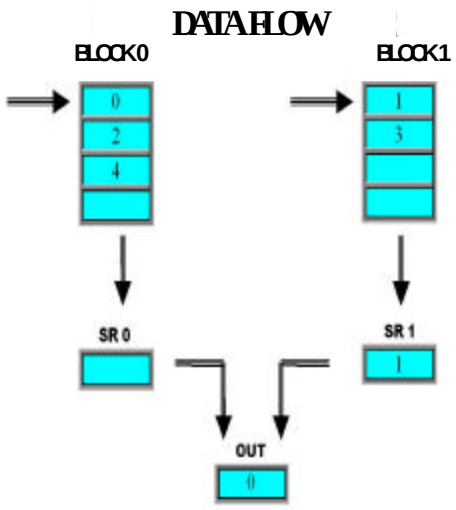


FIGURE 2
DATA FLOW OF PIPELINE FIFO MEMORY

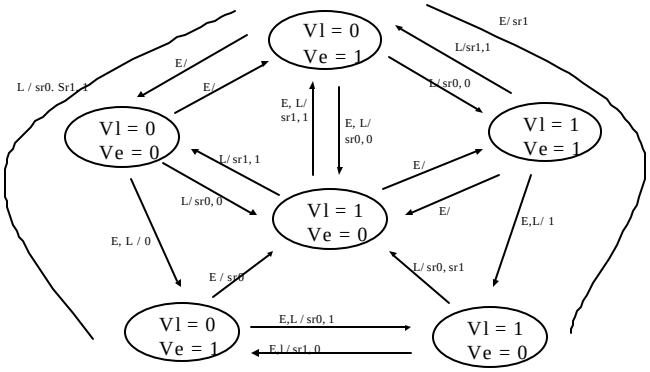


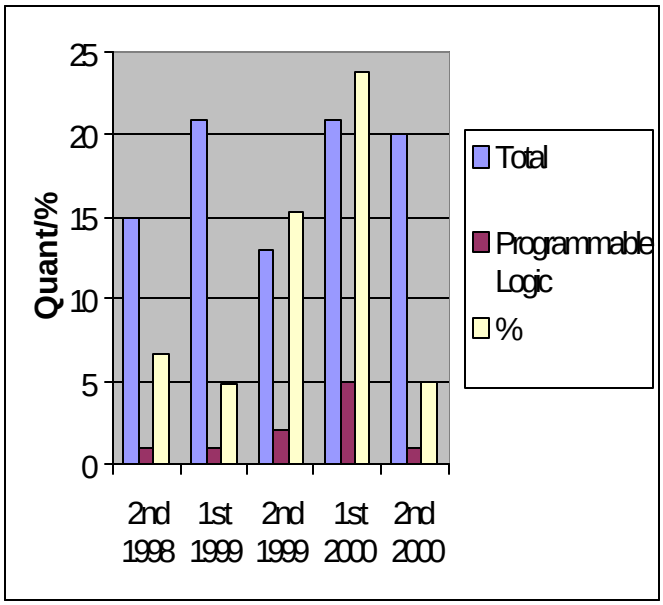
FIGURE 3
STATE TRANSITION DIAGRAM FOR PIPELINE FIFO

The control process can be considered six-state automata, which can be represented by a transition diagram (figure 3). The ellipses characterize state (Vl, Ve and P) and indicate in which block R/W should take place or there is a penance. Arrows indicate synchronous transitions, according to the states E and L, which are external write and read request respectively and shown on the diagram. In the same inscription, the actions to be taken are identified after the bar. Sr0 and Sr1 mean transfer of the corresponding memory block to these registers, while the indices 1/0 indicate which of them will be selected to for output. The implementation was done in VHDL and it was divided in two parts: an asynchronous one for flag generation, and a synchronous one for data transfer and state variables upgrading. The code was compiled, simulate and tested in hardware using tools (MaxPlus II) and devices (Flex 10K20) from Altera Corp.

FINAL TERM PROJECTS

The Final Term Project is a curricular activity in FEI. In the same way it has occurred in Scientific Initiation Program, the existence of VHDL Group not only contributed to improve the digital systems design methods, but also made grow the amount of students who choose programmable logic as the technological solution for their designs. The graph presented in Figure 4 shows given statistics on the evolution of amount of designs that used this technology, over total number of designs since 1998.

FIGURE. 4
PROGRAMMABLE LOGIC IN FINAL TERM PROJECTS



On qualitative aspect, we can also see advantages. Some of presented designs achieved degrees of sophistication that would not have been possible without the use of a formal hardware description language as VHDL. Many designs included FPGA components of up to 100,000 logic gates. The following text describes one of Final Term Projects which had some members of VHDL Group included in design team. The project is named Autonomous Vehicle Control System (AVCS). The objective was controlling an industrial transport vehicle without direct interference of operator that would be applied to restricted area facilities where object transportation was necessary, as ports, airports or any another kind of facility. The vehicle should not depend on tracks and should be guided through simple painted marks on the floor. Paths should be determined by

specific software. Communication should be implemented through radio-frequency links. This choice would avoid use of cables.

The implemented solution is divided in two subsystems:

- Location and path determination subsystem; and
- route control, where students applied the knowledge developed in VHDL Group

Location and path determination subsystem is played by a PC type computer, with software capable to choose a path, based on facility geographic features and historic log. Computer also commands whether vehicle must enter in operation or not. Figure 5 illustrates main operation screen.

Route control subsystem is located, in contrast of location and path determination subsystem, inside vehicle. The whole subsystem is implemented in just one Altera Corporation FPGA device, due to real time and low cost requirements. Digital design is, of course, described in VHDL. This subsystem is in charge receiving the order from computer, processing this information, returning vehicle status to computer, initiating vehicle movement, controlling and processing information given by a CCD device with which it reads guiding marks made on the floor, and finally controlling through pulse width modulation outputs, traction and direction DC motors.

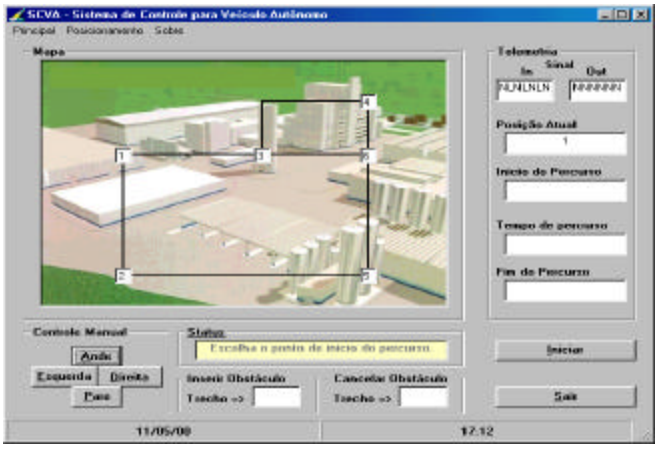


FIGURE.5
LOCATION AND PATH DETERMINATION SUBSYSTEM MAIN SCREEN

Prototype

A prototype was assembled in scale. An optical assembly, including a mirror and some lenses couple optically CCD device to ground image. Figure 6 shows prototype in movement, following a pen traced line. The position of the line in relation to CCD image, used in digital proportional control can be seen in a display located under the vehicle platform.

This project was presented in FEI´s XIX Final Term Project Exposition and became of interest of most entrepreneurs invited.

The involved students, at this time Electronic Engineers occupying positions in industry, recognize participation in VHDL Group as an important activity that influenced not just the technological Final Term Project solution, but their professional choices and development.

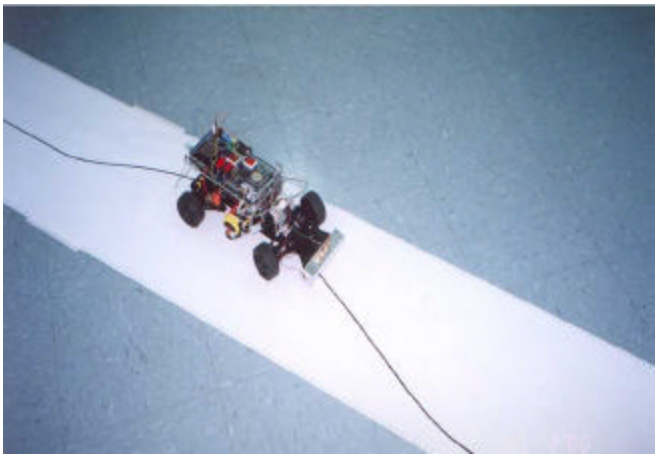


FIGURE.6
PROTOTYPE IN MOVEMENT

CONCLUSION

It was verified that non-curricular disciplines, involving formative issues, but still connected with industrial activities, stimulate students and open new perspectives in other academic and professional activities. It was also noted that the course was successful because of its industrial appeal, contributing with a more professional character, rather than an academic one. Students could perceive an opportunity for distinction among their colleagues and felt attracted by the possibility of effective industrial applications.

The freedom offered by the absence of a formal and conventional way of evaluation emphasized the sense of responsibility and maturity of the participants, making them feel committed and, at the same time, achieving the expected results.

The creation of the VHDL group contributed significantly to increase the interest of students for specific areas, and induced them to elaborate projects not only as an intellectual and technological exercise, with possible future academic perspectives, but also as a professional technical differential to be competitive for future placement in industry. Part of the course was implemented in the regular program, in laboratory activities.

Extra-curricular courses give the necessary diversity and flexibility to bring complementary knowledge in the academic world, contributing for professional formation for world market.

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