PROGRAMMABLE ANALOG INTEGRATED CIRCUIT FOR USE IN REMOTELY OPERATED LABORATORIES

Carsten Wulff[1], Trond Ytterdal [2]

Abstract — The work presented here aims to outfit remotely operated laboratories with circuit programmability through the use of a programmable analog integrated circuit. A concept for remotely operated laboratories using programmable analog integrated circuits is presented. The architecture for a programmable analog integrated circuit and top-level simulations are described.

Index Terms ¾ Programmable analog integrated circuit, remote laboratory, circuit programmability.

INTRODUCTION

Laboratory experience is essential when educating designers of analog (and digital) integrated circuits, providing a base for intuitive understanding of the underlying theory. The test equipment for analog integrated circuits is often expensive, and to equip a lab to serve 30 students is impossible for most universities. Remotely operated laboratories provide a cost advantage in centralizing test equipment while providing students with decentralized concurrent access. Remotely operated laboratories have been explored in [1]-[5], [12]. Already there are remote laboratories that enable a student to make measurements on integrated circuits over the Internet. These laboratories often have a limitation on what types of integrated circuits or devices the student has access to. Some labs [10] have large switching matrixes so the student can select from different circuits to measure, others have a single integrated circuit with some tunable parameters [11], [12]. We propose to take different approach to solve this limitation. Instead of using expensive switching matrixes, we aim to use a programmable analog integrated circuit to provide a lab with circuit programmability. We will start by introducing the concept of programmable analog integrated circuits and the system architecture, then a description of the chip architecture and simulations.

CONCEPT

We will first explain the concept of programmable analog integrated circuits for those readers unfamiliar with the subject, and then describe the concept for the system architecture.

Programmable analog integrated circuits

The concept of a programmable analog circuit can simply be described as having an integrated circuit with "standard" cells that can be wired into an analog circuit i.e. a filter or an amplifier. Figure 1 shows an example of a programmable analog circuit. By controlling a routing network, which can connect the analog cells to each other, we can "build" analog circuits. In the figure the two resistors and the operational amplifier are connected together to create an amplifier with gain A=-R2/R1.

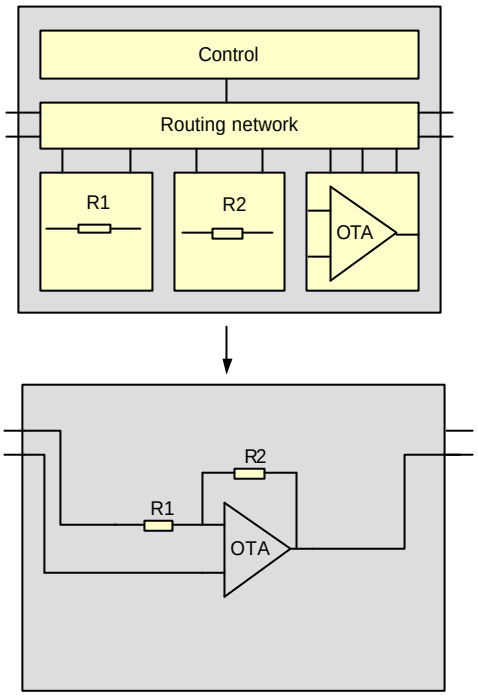

FIGURE 1 PROGRAMMABLE ANALOG INTEGRATED CIRCUIT EXAMPLE

Programmable analog integrated circuits have been reported for more than a decade [6]-[9]. Several manufactures have made programmable analog integrated circuits, among these are; Motorola, IPM Inc, Lattice and Anadigm. Several designs of Field Programmable Analog Arrays (FPAA) have been reported [6]-[7], but these are often aimed at a commercial market as an analog counterpart to Field Programmable Gate Arrays (FPGA) for rapid

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prototyping of analog circuits. The marked for these FPAA circuits has not gained the same momentum as FPGA. This is probably because of the much greater challenges involved in creating a programmable analog integrated circuit. One of the main challenges in creating FPAAs is the fact that analog circuits do not have a smallest common denominator. Digital circuits can (in theory) be created from NAND gates no matter the complexity of the circuit. One approach to circumvent this obstacle is to create expert cells [8]-[9], where each analog cell has a set of tunable parameters i.e. a filter with tunable cut-off frequency. These expert cells are designed by analog designers and are guaranteed to operate within specification. It is a modification of the expert cell approach that has been taken with our Programmable Analog Integrated Circuit (PAnIC).

System Architecture

An overview of the system architecture is presented in Figure 2 and Figure 3. A web-server is connected to a microcontroller and instruments. The instruments can range from simple multi-meters to expensive network analyzers. The instruments are connected to a circuit board that holds several PAnIC chips. Each PAnIC has a set of analog cells that can be selected alone, or wired together to create a more complex circuit. A student connects to the web-server and gets a graphical user interface that contains a toolbox with the available analog cells. The student draws a circuit from the analog cells in the toolbox and submits the circuit to the web-server. The web-server configures the PAnIC chips, through the microcontroller, to create the circuit the student requested. It then performs measurements on the circuit the student has drawn and returns the result to the student.

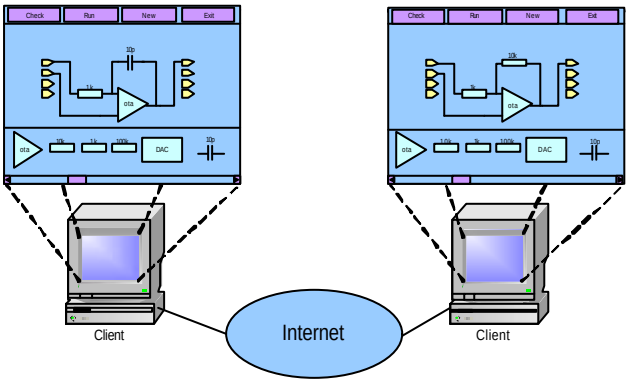

FIGURE 2. SYSTEM ARCHITECTURE: CLIENT

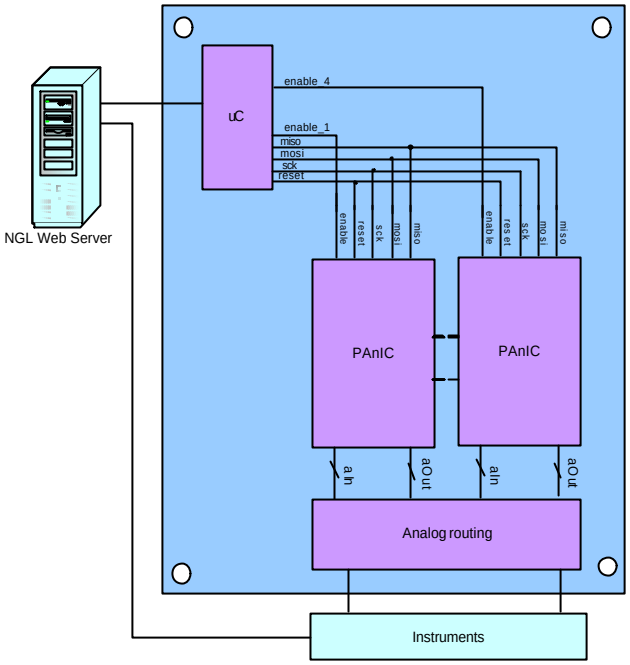

FIGURE 3. SYSTEM ARCHITECTURE: SERVER-SIDE

PANIC ARCHITECTURE

The PAnIC is based on the ideas published in [8], [9]. The PAnIC consists of control logic, an analog module framework (AMF) and several analog cells. A block diagram is pictured in Figure 4. The PAnIC can be interfaced with most microcontrollers and provides 4 analog input signals and 4 analog output signals.

Control

Control consists of a serial peripheral interface (SPI), address register, control signal decoder, module address decoder and a table of content. The SPI is used for data and address communication with the microcontroller. The module address register and decoder are for addressing the analog modules (analog module is the analog cell plus the analog module framework). The PAnIC architecture can address up to 16 analog modules, but in the prototype we chose to only implement 6. The table of content stores an identification tag for each analog module such that a user does not need to know the address of i.e. the differential comparator to use it. When the system starts it can read the table of content and find the module address that correspondes to the desired analog cell.

Analog module framework (AMF)

The AMF consists of; input register & switch (IRS), output register & switch (ORS), line decoder and module register. The IRS serves as input for the analog module, each IRS can switch up to 8 signals in any combination and each AMF can have up to 5 IRS cells. In addition the IRS provides a function denoted ReadBack that is essen-

tial in the design and will be explained later. The ORS cells provide buffering of the output and can switch the output signal to one (or none) of 4 off-chip output signals. Each AMF has two ORS cells. The module registers servers as an 8-bit digital input and output. It can also be used for control signals for the analog cell. The line decoder provides an enable signal for each of the IRS, ORS and module register.

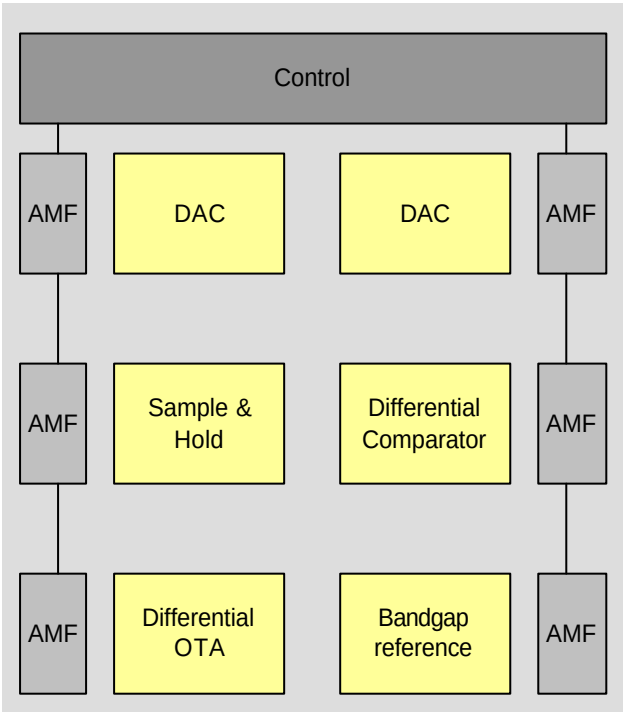

FIGURE 4 PANIC ARCHITECTURE

Analog Cells

The analog cells in the prototype consist of a Digital to Analog Converter (DAC), sample & hold, differential comparator, differential operational transconductance amplifier and a bandgap voltage reference. Students in the course Analog CMOS 2, at our university, have designed all analog cells in the prototype. The types of cells are all frequently used in application specific integrated circuits (ASIC). The different ways the cells can be connected is all predetermined during layout of the chip. A possibility for a connection is made by connecting and output signal from an ORS to an IRS of another cell. One of the circuits that can be created with the prototype is an Analog to Digital Converter (ADC). By connecting the DAC, sample & hold and the differential comparator as pictured in Figure 5 we can construct the analog portion of a successive approximation analog to digital converter. An ADC of this type performs a binary search to find the binary output word that most closely resembles the analog input value. It first compares the input value to ½ the signal swing, if the input value is higher the most significant bit (MSB) is 1, if the input is lower MSB is set to zero. It then continues in the half that it knows the input signal lies within, After 8 comparisons the correct digital output word within a resolution of 8 bits is found. The successive approximation register, which controls the binary search, is modeled in the micro-controller.

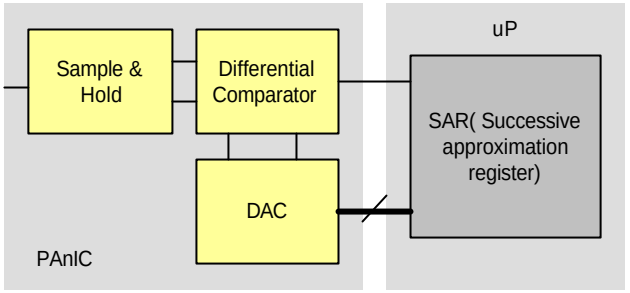

FIGURE 5. ADC BLOCK DIAGRAM

ReadBack

ReadBack is, as mentioned, an essential part of the PAnIC design. ReadBack provides a system using the PAnIC chip with a method to discover how to connect the analog cells together and which connections are possible. When the system starts it can request from the PAnIC a “list” of all possible connections between the analog cells. This in combination with the table of content makes the PAnIC a self-consistent programmable analog integrated circuit for use in a flexible environment such as a remote laboratory.

SIMULATION

A model for the PAnIC was initially constructed in SystemC [13] to test the validity of the concept. Simulation of the PAnIC was done at all levels but especially on circuit programmability, SPI, ReadBack and the Analog to Digital Converter. The simulation results verified that the concept vas valid. The SystemC model was translated into VHDL for the digital portions, and the analog portions (switches, analog cells and buffers) were modeled in SPICE. The VHDL model was simulated using both a behavioral representation and synthesized netlists using process specific cells. In all simulations, the PAnIC has preformed as expected.

CONCLUSION

The use of programmable analog integrated circuits in remotely operated laboratories has been introduced. The architecture of PAnIC has been explained and proven through simulations to be a self-consistent programmable analog integrated circuit. The PAnIC provides a remote

laboratory with extended flexibility through circuit programmability.

FUTURE WORK

The PAnIC is in the last stages of the design phase and the prototype will go into production august 2002. A prototype remote laboratory using the PAnIC is scheduled for end of 2002 beginning of 2003.

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