Electronics Packaging – A Course for Rutgers University School of Electrical and Computer Engineering

Michael F. Caggiano[1], Ka M. Ho[2]

***Abstract** -- In this talk, I will profile one of the modules of a course that is being developed as a Web-based enhancement of a new graduate course entitled "Electronics Packaging". The course, developed and introduced into the ECE Department at Rutgers University during the spring of 2001, deals with the electrical characterization and modeling of the parasitics for integrated circuit packaging. The module being profiled is one on the package effects on signal integrity. The whole course is targeted at the electrical engineering population of full-time students and industry part-time graduate students that have a background in circuit analysis. In this presentation, I will discuss the status of the course and demonstrate a sample of the Web designed lectures related to signal integrity.*

Index Terms – Electronic packaging, electrical analysis, education.

INTRODUCTION

Communication systems and information processing systems require IC's that need to combine the attributes of low power consumption, good performance and small size. To meet this performance challenge, as well as adding features to shrinking system sizes, the system interconnect of packaging will have a paramount effect on signal integrity and chip to chip communication speed. Package inductance, capacitance, mutual inductance and mutual capacitance will affect the rise times, fall times, resonances, generate spurious oscillations and introduce noise and delays into the systems.

Courses offered in major universities that address packaging are typically in the department of Mechanical Engineering. These courses cover the materials and thermal properties of packaging. The proposed course will be in the Electrical and Computer Engineering department and will deal with the electrical characterization and modeling of the parasitics of integrated circuit packaging. The motivation of the proposed course is to introduce the concepts of analyzing and electrically modeling the IC package parasitic effects and to investigate the impact these effects have on signal speed and integrity for the electronic devices which they house [1]. This course will be of interest to circuit design engineers that need to understand the electrical effects contributed by the package parasitics to their circuit designs. Therefore, the emphasis of the course will be placed on the electrical characterization of packaging rather than the mechanical issues, in order to meet the needs of the circuit designer as well as the package designer. Since packaging contributes 45% of the cost to manufacture an integrated circuit, this course will provide the student audience with an experience that the microelectronics industry will find very valuable in addressing their high speed, high density and low cost IC designs.

COURSE STATUS

Starting in September, 2001, equations, charts, graphs and other figures pertaining to inductance, resistance, capacitance, characteristic impedance and signal integrity were entered into PowerPoint with notes about the topics entered as text beneath the slides. These modules were revised and updated as of May 2002. Samples of the slides for the signal integrity module are presented in this publication. Sample slides for the inductance module were presented in the 5th International Conference on Packaging and Training held in Dresden, Germany in March 2002 [2]. Sample slides for the capacitance module were presented in the 25th International Spring Seminar on Electronic Technology, held in Prague, Czech Republic. Starting in the spring semester 2002, the topics related to modeling, simulations, noise and measurements will be added. These topics will not be covered in this publication but were made available for the oral presentation at the 52nd ECTC conference that was held in San Diego, California in May of 2002. The module units are designed to stand-alone so that the audience would be able to learn any one topic of their choice. The series of modules, if taken in sequence, would provide the audience with a complete course. During the 2002-2003 academic year, the slides will have spoken comments added employing Sync-O-Matic software so that web based streaming lectures can be produced. The total project should be complete and a few CD's available for demonstration by the end of the spring 2003.

[1] Michael Caggiano, Department of Electrical and Computer Engineering, Rutgers University, Piscataway, NJ. 08854-8058, 732-445-0678 (Voice), 732-445-2820 (FAX) cagg@ece.rutgers.edu

[2] Ka M. Ho, Department of Electrical and Computer Engineering, Rutgers University, Piscataway, NJ 08854-8058 vivianho@ece.rutgers.edu

MODULE SYNOPSIS ON SIGNAL INTEGRITY

The conductive paths in the package represent an electrical RLC network to an integrated circuit. Determination of the resistance, inductance, capacitance and both mutual inductance and mutual capacitance would be covered in detail in a different module of the course. In this module, the network of package parasitics will be studied to determine the network's effects on signal waveforms. The topic will start with an analysis of two port networks by first analyzing the wave shaping properties of RC circuits. Then, by adding series inductance to the RC circuit the two port network analysis will now include the transfer function of an RLC circuit. This RLC circuit can be viewed as a two-pole low pass filter. Applying a step function to the circuit will produce an output that will contain a rise time, damping, ringing and overshoots. Signals transmitted through these networks will also contain propagation delays introduced by flight times of the conductors and dielectrics. Circuit simulations of RLC circuits to pulse inputs will give insight to the students on the signal degradation due to the package parasitics. The following figures, excerpts taken from Power Point slides of the module, are presented along with a brief discussion.

Figure 1 shows a simple RC representation of a signal conductor in a package. The resistance is a combination of the generator's resistance and the path resistance. In this case we are assuming that this resistance dominates the inductive reactance of the path so that the inductance is neglected. The response to a step function of the circuit is shown in Figure 2 with output voltage values, as a function of time, given in Figure 3.

RC TRANSMISSION LINES FOR IC PACKAGES :

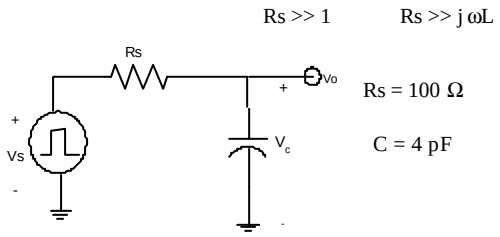


Figure 1. An IC package represented as an RC circuit.

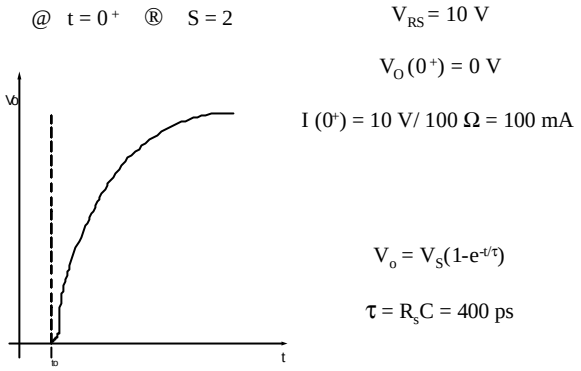


Figure 2. Output voltage waveform for a step input.

When $t = \tau$ (one time constant) $e^{-1} = .37$

and $V_o = 63\ \% V_S$

Other Examples :

$t = 2\ \tau \rightarrow V_o = 86\ \% V_S$

$t = 3\ \tau \rightarrow V_o = 95\ \% V_S$

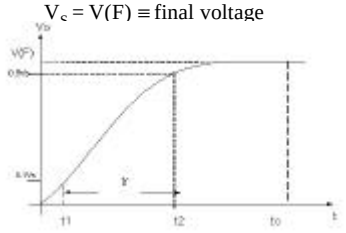
$t = 5\ \tau \rightarrow V_o = .993\ V_S \equiv$ fully charged

Figure 3. Output voltage for various times.

Figure 4 demonstrates a method of determining the rise time for an RC circuit from the values of R and C.

RISE TME FOR AN RC CIRCUIT

$V_e = V(F) \equiv$ final voltage



Rise time is defined as the time it takes to go from 10 % to 90% of the final voltage V(F)

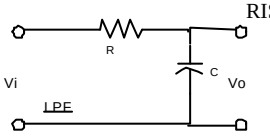
$$t_r = t' = \tau \ln [(V_F - .1V_F) / (V_F - .9 V_F)] = \tau \ln 9 = 2.2\tau$$

$V_F = V_s$

Figure 4. Output voltage waveform of a low pass filter when a step voltage is applied as the input.

An RC low pass filter has a frequency response shown in Figure 5 and a –3dB frequency of f_H. By equating the reactance of X_C to f_H (Figure 6) and the rise time to RC (Figure 4) the relation between f_H and tr can be found (Figure 7).

RELATIONSHIP BETWEEN BETWEEN f_H (3db freq) WITH RISE TIME



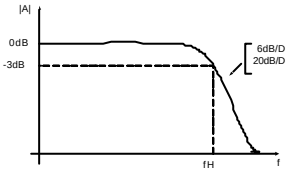


Figure 5. Bode plot for the low pass filter circuit.

$$V_o = V_i (X_C / (R + X_C))$$ complex number volt div.

$X_C = 1 / j\omega C$

$|X_C| = 1 / 2\pi fC$

Define f_H as:

when $f = f_H$ then $Av (f_H) = -3db$ (definition)

or

$V_o = .7\ V_i$ (-3db)

$\therefore\ X_C / (R + X_C) = .7$ (voltage division; in complex numbers)

$\therefore\ R = |X_C| = 1 / 2\pi f_H C$

Figure 6. Determining the capacitor impedance.

$\therefore\ f_H = 1 / 2\pi RC = 1 / 2\pi\tau$ (from previous eq.)

$\tau = 1 / 2\pi f_H = 1 / \omega$

Recall $t = 2.2\ \tau$

$t_r = 2.2 / 2\pi f_H = .35 / f_H$

or

relate t to f

$f_H = .35 / t_r$

$\omega_H = 2.2 / t_r$

for single pole or dominant pole

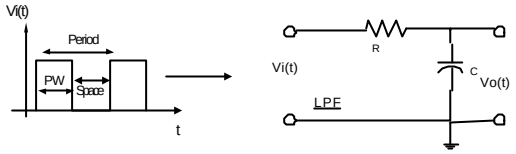
Figure 7. The relation between the –3dB frequency and the rise time for a low pass filter.

Figure 8 shows a package LPF network receiving a square wave as an input. Figure 9 shows the output response to the input at steady state, which occurs after fife cycles when the RC time constant is equal to the pulse width of the waveform.

Steady state response of an RC circuit to a Square Wave

where $\tau \approx$ PW (previous case was PW >> τ step function input)

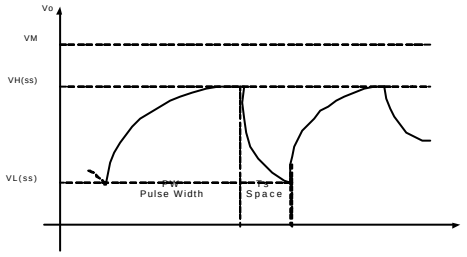
Heavy capacitor loading and large R



Duty cycle =PW/τ *100%

Figure 8. Square wave input to the low pass filter.

@ steady state in 5τ = 5 cycles (PW)

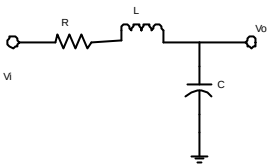


$$V_L(ss) = V_H(ss)e^{-Ts/\tau}$$

$$V_H(ss) = V_M - (V_M - V_L(ss))e^{-PW/\tau}$$

Figure 9. The steady state response of a low pass filter to a square wave input.

When the signal source resistance is small compared to the package inductance, then the inductance plays a role in the low pass filter action of the package network. Figure 10 shows the circuit and its transfer function, H(s). The best way to look at the performance of this circuit is to apply a step function (Figure 11) and then solve for the roots of the denominator of the output voltage Vo(s). Figure 12 shows the time domain output waveform for the under damped case when the roots are complex and conjugates. K is the coefficient of damping, ω_0 is the resonant frequency, ω_d is the ring frequency and T_d is the ring period.



$1/sC = X_C$

$sL = X_L$

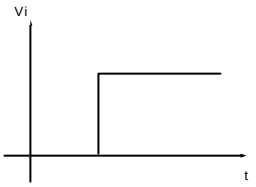
$$H(s) = (1/sC) / [R + sL + (1/sC)] = 1 / [RsC + s^2CL + 1]$$

$$H(s) = 1 / [1 + (RC)s + s^2(LC)]$$

Figure 10. A package conductor represented as a RLC low pass network.

BEST WAY TO ANALYZE A NETWORK IS TO SEE THE RESPONSE TO A STEP FUNCTION

A step input



$V_i(s) = V/S$

$V_o(s) = H(s)V_i(s)$

Solve for roots in denominator of $V_o(s)$

$s_{1,2} = -K\omega_o \pm \omega_o\sqrt{(K^2 - 1)}$

Figure 11. Step input to the low pass filter.

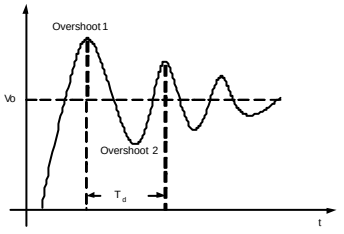
UNDERDAMPED

$$V_o = 1 - ((K\omega_o/\omega_d)\sin\omega_d t + \cos\omega_d t)e^{-K}$$

$\omega_d \equiv$ ring frequency $= \sqrt{(1-K^2)}w$

overshoot $= e^{[-\pi Km/(1-K2)^{1/2}]}$

s_1, s_2 complex and conjugates



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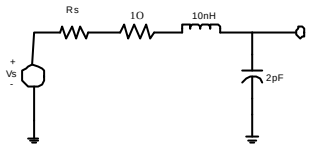
igure 12. Output response of the filter to the step input.

Figure 13 is one of the analysis examples in the module. The figure lists the values for the R, L and C that make up a

conductive path in the package. The object of the example is to determine the ring frequencies, the overshoots of the output waveform. Figure 14 (case 1) is for a severely under damped case while Figures 15 and 16 (case 2) have some additional series resistance however, the network still remains under damped. Figure 17 shows how to solve for the rise time of case 2. Since both cases are for networks that are under damped, they both will have ringing.

EXAMPLE : PACKAGE TRACE



$w_o = \frac{1}{\sqrt{LC}}$ = 7 G Rad f_o = 1.1 GHz

$Q = \frac{\sqrt{\frac{L}{C}}}{R} = \frac{22 \ .3}{1\Omega} = 22 \ .3$

Figure 13. Module example of a package conductor.

Need R = 44.6Ω for critical damp ∴ R_s > 43.6Ω for no ringing

Case 1

R_s = 0Ω Q = 22.3 K = .022

Ring Frequency = $(\sqrt{1-K^2})\, f_o$ = 1.1 GHz

Overshoot 1 = $e^{[-\pi(.022)(1)/(1-.022^2)^{1/2}]}$
= .93
2 = .86

Figure 14. Determination of ring frequency and overshoots for case 1.

CASE 2

$R_s = 9\Omega$ $Q = \frac{22.3}{10}$ = 2.2 K=.22

Ring Frequency = $(\sqrt{1-(.22)^2})\, f_o$ = 1.07 GHz

$T_R = \frac{1}{1.07GHz}$ = 931ps

$T_R = \frac{1}{f_R}$ = 931 ps Ring period

Figure 15. Determination of ring frequency of case 2.

Overshoot = $e^{[-\pi Km/(1-K^2)^{1/2}]}$

K = .22 m = 1 overshoot 1 = .5

V = 1 + overshoot 1 = 1.5

m = 2 overshoot 2 = .24

m = 3 overshoot 3 = .12

Figure 16. Determination of overshoots of case 2.

Rise time t_r : measured from 10% to 90% of V_o

$\phi(10\%)$: sin $\phi_{10\%} = \frac{.1}{1.5}$ $\phi_{10\%}$ = 4°

$\phi(90\%)$: sin $\phi_{90\%} = \frac{.9}{1.5}$ $\phi_{90\%}$ = 37 °

$\phi(90\%) - \phi(10\%)$ = 33 °

360 ° represents a full wave = 931 ps f(ring)

$\frac{33°}{360°}$ represents .092 of a full wave

t_r = (.092) (931 ps) = 85.6 ps

Figure 17. Determination of rise time of case 2.

CONCLUSIONS

Electrical circuit analysis and modeling of IC packages are necessary to accurately simulate the response of the assembled device. While models of discrete components are readily available from manufacturers, models of integrated circuit packages containing reactive parasitics are much harder to obtain. Many companies do not have the resources to purchase expensive software or dedicate and train staff for this task. There needs to be a generation of academically trained IC circuit designers that have an understanding of the performance degradation that the IC package produces.

This course is a tutorial on the methods of analyzing an IC package and determining its electrical characteristics. It starts with providing the student with the theory and equations necessary to analyze and model various types of packages [4,5].

Excerpts from the signal integrity module of the course are presented in this paper to give the audience a sampling of the course material. Course slides, with portions of the accompanying text, are presented to demonstrate the material. The remaining part of the course addresses the electrical characterizations of packages and the necessary tools needed to create a computer program that would generate electrical models of packages [6]. Also covered in the course are the techniques for verifying the simulation models that were studied in earlier parts of the course.

Chip packages play a large role in the performance of high performance processing IC's and the knowledge gained in this course would provide a useful tool for a design engineer.

References

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