Bridging to Practice in Computer Engineering Education

J. Morris Chang
Computer Engineering Program and Dept. of Computer Science
Illinois Institute of Technology
10 west 31st street, Chicago, IL 60616
Internet: chang@charlie.iit.edu

Abstract

In order to bridge the gap between the academic abstraction and the industrial practice in Computer Engineering (CPE) education, attempts have been made at Illinois Institute of Technology to teach the students "the way they will work". Three major areas are addressed — (1) System Design Using Commercial Tools, (2) Integral Process of Design and Test and (3) Inter-Professional Interaction. This short paper presents the approach taken and the experience gained from therein.

1. Introduction

Over the past 15 years, dramatic improvements in VLSI technology have fueled a computer revolution. Large, expensive mainframe computers have been replaced by small, inexpensive, high-performance workstations and personal computers that are used in nearly all aspects of business and education. This drastic technology advance enables many of today's exciting new applications, including interactive multimedia, and high-speed computer networks. The development of these applications requires engineering professionals with skills in both hardware and software design. The discipline of Computer Engineering (CPE) addresses this need.

In response to the strong demand of computer engineers from industry, many universities have expanded their CPE programs in the past decade. Moreover, the rapid technology advance —the driving force makes technology become more and more affordable — also calls for a constant modification to the CPE curriculum in order to bring it up to date. We all face the challenge in how to bridge the academic abstraction to the industrial practice in such a dynamic environment.

This paper addresses our approaches in bridging to practice in computer engineering education. Our approaches include: (1) system design using commercial tools, (2) integral process of design and test and (3) inter-professional interaction. We believe that these three key components are crucial to today's CPE program. These approaches will teach our students "*the way they will work*".

Partial support for this work was provided by the National Science Foundation's Division of Undergraduate Education through grant DUE-9650347

2. System Design Using Commercial Tools

Recent advances in VLSI technology can be described through the development of Intel's 80x86 architecture shown in the following Table. This technology trend closely follows the famous Moore's law (circuit density doubles every 18 months or so).

Table 1: The development of Intel's 80x86 architecture

Year	1985	1990	1993	1995
CPU	386	486	Pentium	P6
number of transistors	275K	1.2M	3.2M	5.5M

Although the principles of digital system design remain unchanged, the complexity of design has grown substantially. To cope with the increasing complexity, we introduce the industrial standard hardware description language —VHDL (IEEE 1076) into our digital systems design courses [1, 2, 3].

Students get familiar with a widely used commercially available VHDL tool - *Maxplus2* (from Altera) through weekly hands-on laboratory assignments. While the laboratory assignments cover the basic principles of digital systems design, students are also gaining experience in the latest CAD tools. This allows us to place a typical design course in the context of modern design methodologies.

Combining VHDL and logic synthesis allows our students to focus on a high level abstraction in digital systems and leave the detailed implementations to CAD tools. Mastering this enabling technology not only makes it possible to design a CPU as the final project in a senior level course but also gives our students an edge in the job marketplace.

It is worth noting that the VHDL tools we used are still evolving (the VHDL tool in *Maxplus2* was introduced in late 1994). Within the past two years, new features were introduced, through latest software release, almost every quarter. For example, the VHDL constructs — *generic* and LPMs were not fully supported until the middle of Spring 1997. In addition to the software upgrade in the laboratory, course notes must be constantly updated with the latest materials. This creates an exciting and dynamic learning environment for both the teacher and the student.

3. Integral View of Design and Test

The ABET Engineering Criteria of US requires a "major meaningful design experience" in all the engineering programs. As a result, design experience is generally addressed in senior courses. However, in a typical product development cycle, testing process usually follows the design process closely. Moreover, as the complexity of digital circuits increases continuously the cost of device testing has also increased sharply. The increasing complexity of testing has shifted more and more of the testing responsibility towards the design engineer. Today, many of the testing strategies must be planned during the earlier design phase. We believe that the integration of test with design is an important attribute within the ability spectrum of a modern day undergraduate computer engineering student.

We have started introducing the various issues and corresponding techniques employed in testing in our digital design courses. These courses include VLSI design course (at circuit level), digital systems implementation course (at board level) and design of microprocessor course (at CPU level). To give this idea a practical perspective, we are in the process of developing an innovative laboratory for linking design and test through hands-on experiments. Students are asked to be *responsible designers* who would perform the testing for their own designs.

To address this emerging need, a laboratory with CAD tools and testing facility is essential. However, the cost of a modern Automatic Test Equipment (ATE) currently used by the industry is in the range of multi-million dollars which is beyond the budget of most of teaching labs. At IIT, we are building a *Virtual* ATE which is based on off-the-shelf components (e.g. Logic Analyzer and Pattern Generator) and promises to be an affordable and innovative solution for university engineering departments.

The *Virtual* ATE effectively simulates the operation of a real ATE in the lab. With this *Virtual* ATE, students can test and validate actual chips or even boards built from their designs. Many of the testing techniques such as DFT (Design for Testability), BIST (Build-in-Self-Test) and Boundary Scan (IEEE 1149.1) are covered in the classroom and also practiced from the design phase through the final testing by students in a single laboratory. This approach not only offers our students the hands-on experience, but also provides them with an integral perspective of the design of digital systems.

Our goal is to develop a continuum of courses which teach undergraduate students that design and test are inherently intertwined in digital systems. Currently we are developing this lab with support from NSF and IIT.

4. Inter-Professional Interaction

At IIT, we believe that the ability to work with different professions in a project-oriented setting is critical to today's engineering education. InterProfession (IPRO) projects (a three-credit course) are integrated into our curriculum. In Spring 1997, one project which involved nine students from four different majors was led by the author. This project was to construct the *Virtual* ATE mentioned in the last section and study other engineering-related issues (e.g. cost/features analysis).

At the beginning of this project, the instructor gave the project overview and led the discussion (brainstorming) with students to identify the tasks. Then, we went through following phases in the semester.

- *Organization Phase*: Once the tasks were identified, students were asked to adopt responsibility according to their interests. Three subgroups were formed: business group, hardware group and software group. Later, a leader emerged from each group quite naturally. Communication protocols (including subgroup meeting schedule) were defined.
- *Preparation Phase*: Vendors were invited to classroom to give presentations and demonstrations about their hardware and software products. Students studied the products left by vendor for evaluation purpose.
- *Exploration Phase*: Problems and roadblocks along the exploration were discussed during meetings. In addition to frequent calls and emails to vendors for the technical support, a conference call was made to the factory engineers, to obtain answers for the critical path.
- *Prototyping Phase*: Finally, a working prototype which combined software and hardware was presented in IIT's Undergraduate Research Conference. Written documentations and oral presentations were delivered.
- *Evaluation Phase*: Each subgroup was asked to evaluate their own work (including the products they used) and report their findings to the entire group. Questionnaires and FAQ (Frequent Asked Questions) were established on the web.

The coordinations and interactions among subgroups and group members are the key factors of the success in this project. More than 300 emails were generated among students. All the documentations are preserved in one web site — http://www.iit.edu/~iddt.

Students are proud to see the working prototype and appreciate much experience in teamwork, project management (i.e. deadlines) and leadership. It is worthwhile to mention that this project received the highest award, "Overall Excellence Award" (with 500 dollars cash prize), among 36 projects participated in IIT's second annual Un-

dergraduate Research Conference, April 18, 1997.

5. Conclusions

The rapid changes in computer technology lead to many exciting new applications in our life. While these computer-based applications are becoming more and more affordable, such product's life cycle is getting shorter. Today's computer engineering educators must recognize this rapid changes and serve as the bridge between academe and industry.

This paper summarizes our approaches in bridging to practice in CPE education. We have examined various degree programs and have found that such an offering is very rare in undergraduate curriculums and once we have demonstrated a successful scheme, it will be readily emulated elsewhere.We are still in the beginning stage of implementing these ideas into our CPE programs. Suggestions and comments are always welcome.

6. References

[1] J. M. Chang, "From VHDL to CPLD - a Synthesizable Journey," workshop presented in IEEE International ASIC Conference, Austin, Texas, Sept. 21, 1995.

[2] J. M. Chang, "Teaching Top-Down Design using VHDL and CPLD," *Proceedings of IEEE Frontiers in Education Conference*, Salt Lake City, Utah, November 6-9, 1996.

[3] J. M. Chang, "Teaching Microprocessor Design and Test," to appear in the *Proceedings of IEEE Frontiers in Education Conference*, Pittsburgh, PA, November 5-8, 1997

7. Biography

Morris Chang received the B.S. degree in electrical engineering from Tatung Institute of Technology, Taiwan, the M.S. degree in electrical engineering and the Ph.D. degree in computer engineering from North Carolina State University in 1983, 1986 and 1993, respectively.

He was an analog IC designer at Texas Instruments, Dallas, Texas, from 1983 to 1984. From 1986 to 1988, he was a Member of Technical Staff at the Microelectronics Center of North Carolina, Research Triangle Park, North Carolina. From 1988 to 1990, he was a Member of Technical Staff at AT&T Bell Laboratories, Allentown, Pennsylvania. From 1993 to 1995, he was an Assistant Professor in the Department of Electrical Engineering at Rochester Institute of Technology, Rochester, NY. In 1995, he joined the Department of Computer Science at Illinois Institute of Technology, Chicago, IL, where he is currently an Assistant Professor.

His research interests include computer architecture, object-oriented programming languages, hardware description languages, memory management and VLSI systems. Dr. Chang has been serving on the technical committee of IEEE International ASIC Conference since 1994. He also served as the Secretary and Treasurer in 1995 and the Vendor Liaison Chair in 1996 for the International ASIC conference.